

APPROVED	Q.G. FIG. 2	
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FIG. 1
(PRIOR ART)

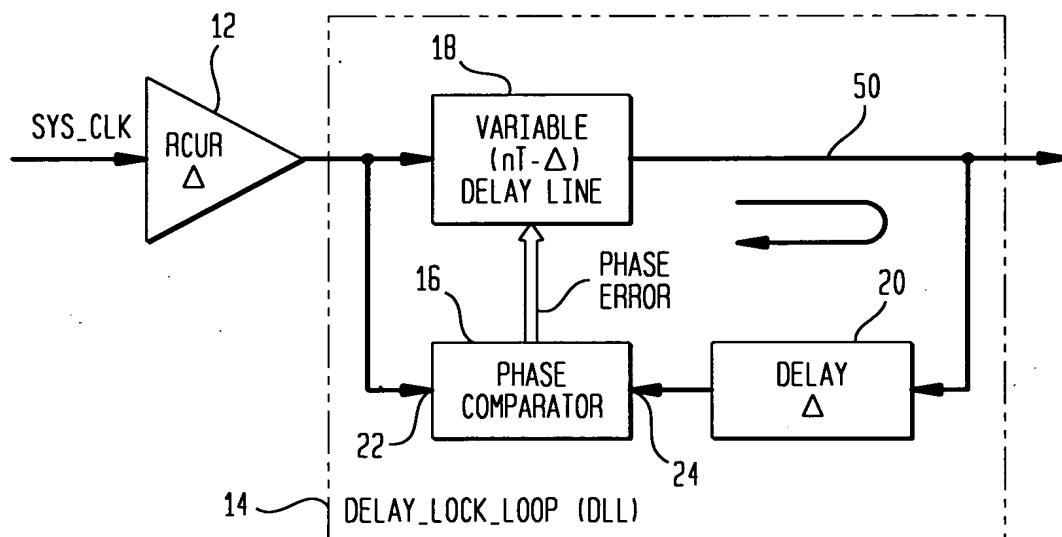


FIG. 2

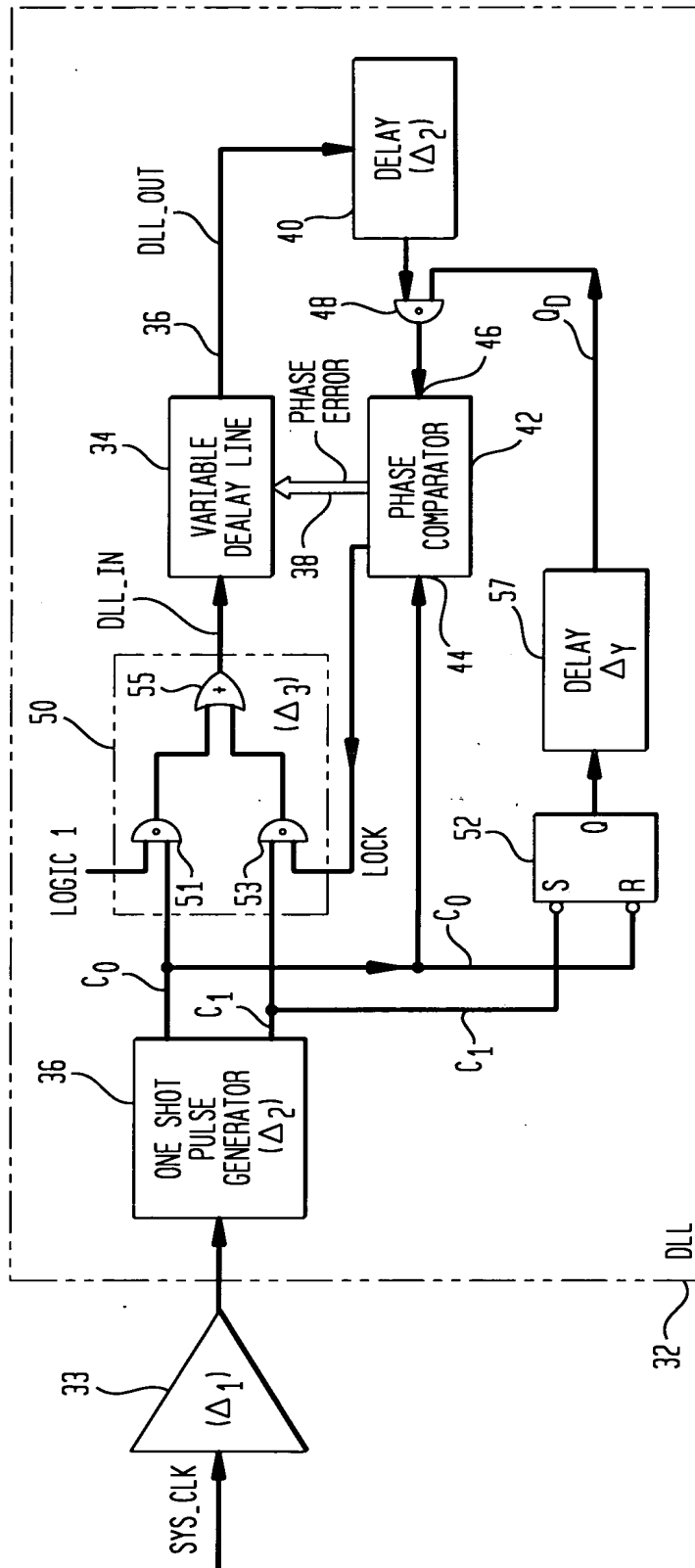


FIG. 3

The diagram shows the following signals and their characteristics:

- FIG. 3A SYS_CLK**: A periodic square wave with period T . A specific pulse is labeled D_1 .
- FIG. 3B RECEIVER 34 OUTPUT**: A square wave with period T . A specific pulse is labeled D_2 .
- FIG. 3C C_0** : A square wave with period T . A specific pulse is labeled D_2 .
- FIG. 3D C_1** : A square wave with period T . A specific pulse is labeled D_3 .
- FIG. 3E DLL_IN**: A square wave with period T . A specific pulse is labeled D_3 .
- FIG. 3F DLL_OUT**: A square wave with period T . A specific pulse is labeled $D_1 + D_2 + D_3$.
- FIG. 3G SIGNAL AT PHASE COMP PORT 46**: A square wave with period T . A specific pulse is labeled $D_1 + D_2$.
- FIG. 3H LOCK**: A square wave with period T . A specific pulse is labeled D_4 .
- FIG. 3I Q_D** : A square wave with period T . A specific pulse is labeled D_4 .

The diagram also includes the following labels and annotations:

- 31**: Label for the period T of the SYS_CLK signal.
- 33**: Label for the period T of the RECEIVER 34 OUTPUT signal.
- PHASE ERROR**: Label for the phase error between the DLL_OUT and the SIGNAL AT PHASE COMP PORT 46.
- ZERO PHASE ERROR**: Label for the zero phase error between the DLL_OUT and the SIGNAL AT PHASE COMP PORT 46.
- $\Delta L = T - (D_1 + D_2 + D_3)$** : Label for the phase error between the DLL_OUT and the SIGNAL AT PHASE COMP PORT 46.

$$\Delta L = L - (D_1 + D_2 + D_3)$$

PHASE
ERROR

FIG. 3H
LOCK

FIG. 31